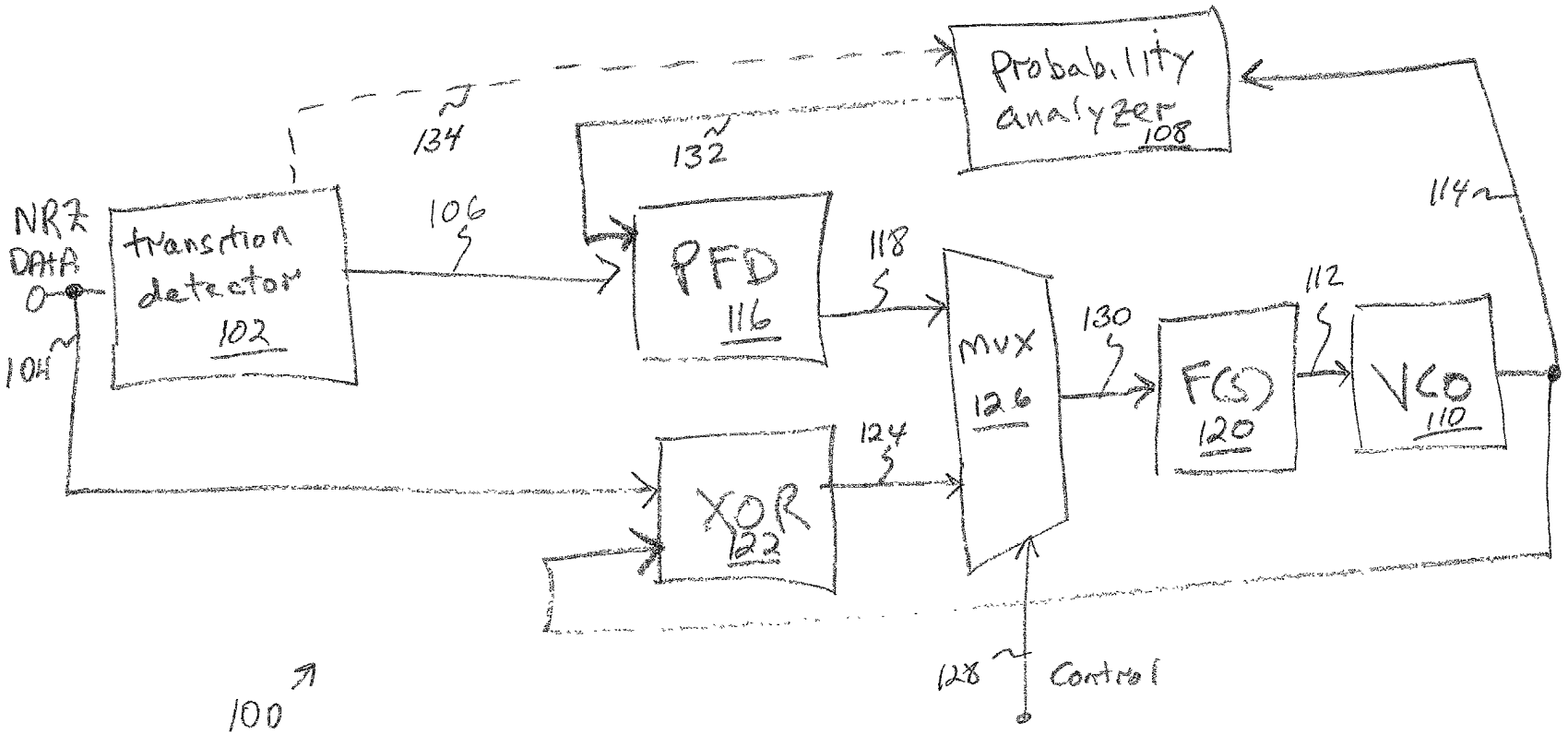
Probability analyzer 108
134
132
NRZ DATA
104
transition detector 102
106
PFD 116
118
MUX 126
130
FCO 120
112
VCO 110
114
XOR 122
124
128
Control
100

Fig. 1

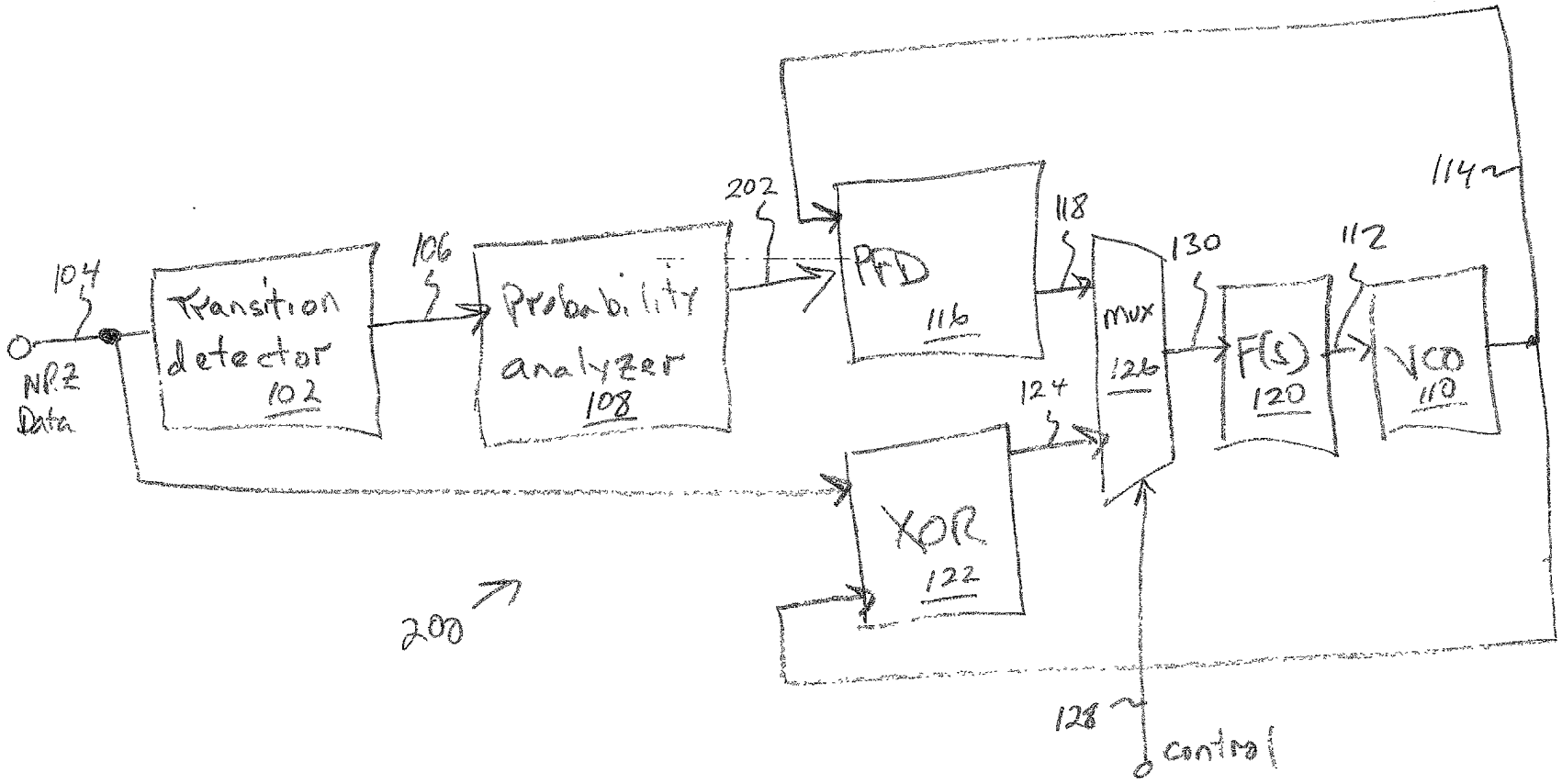
114
202
118
130
112
104
106
Transition detector 102
Probability analyzer 108
PFD 116
mux 126
F(s) 120
VCO 110
NRZ Data
124
XOR 122
200
128
control

Fig. 2

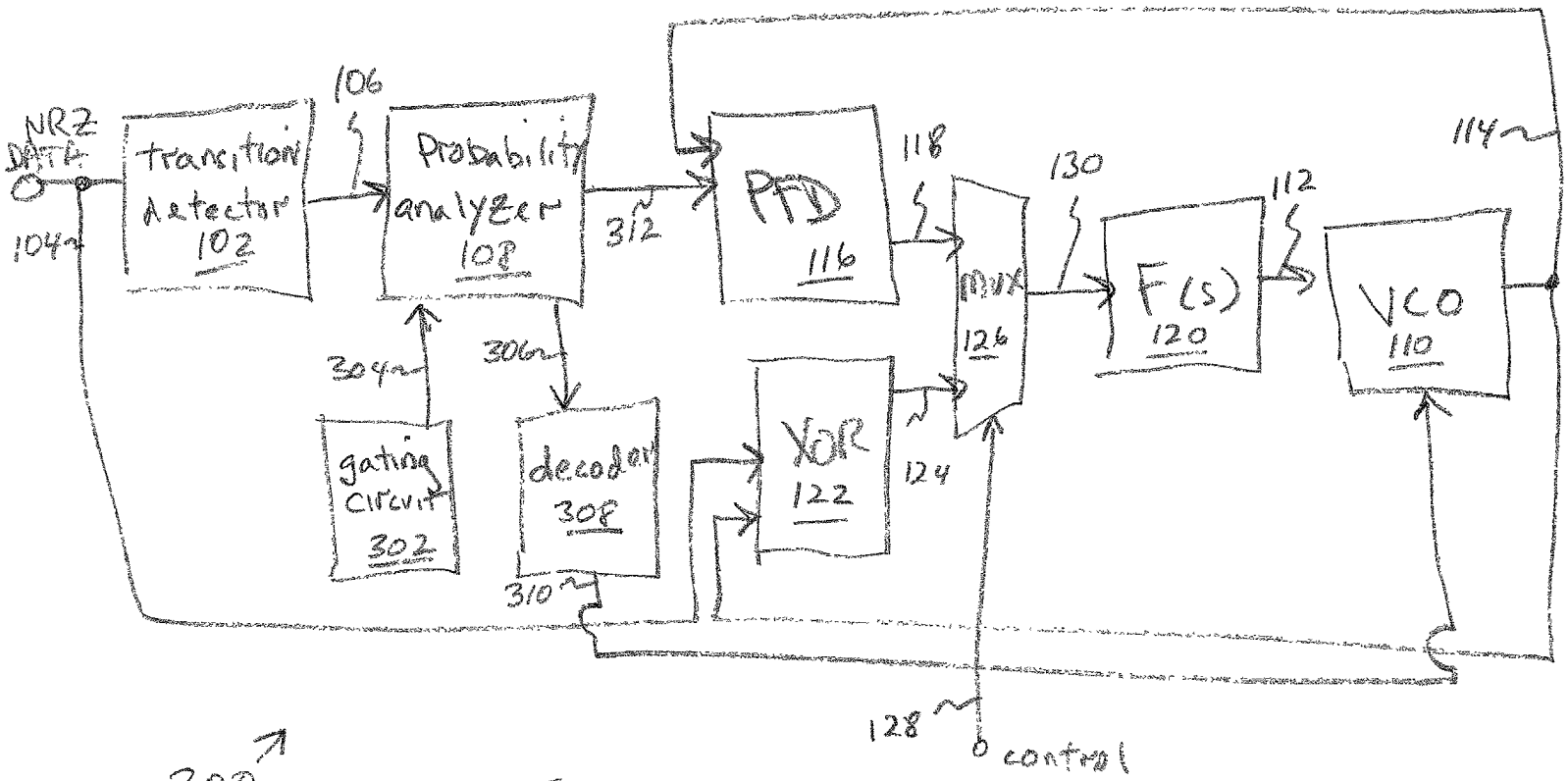
NRZ DATA
104
transition detector 102
106
probability analyzer 108
312
PFD 116
118
MUX 126
130
F(s) 120
112
VCO 110
114
304
306
gating circuit 302
decoder 308
310
XOR 122
124
128
control
300

Fig. 3

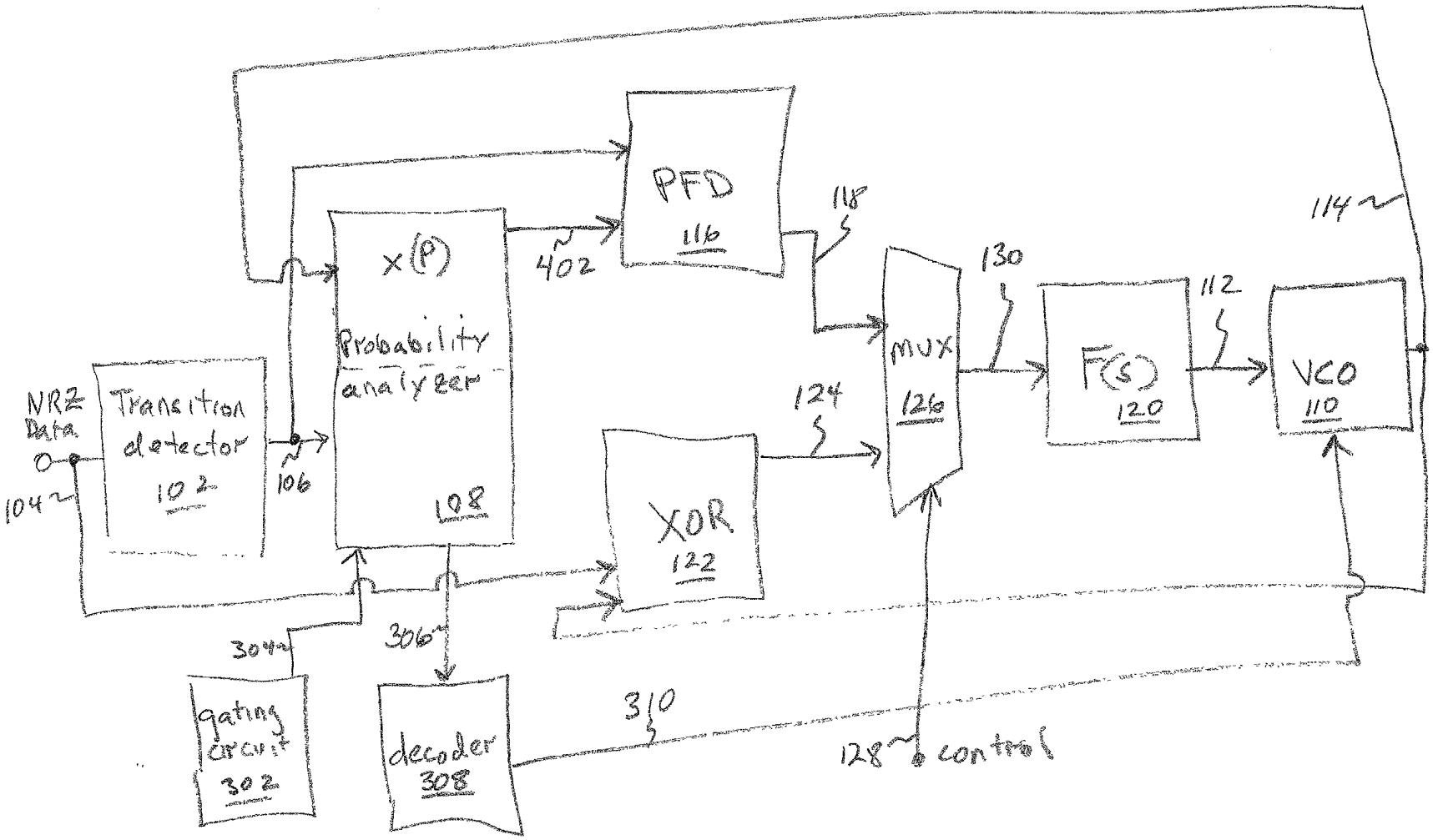
PFD
116
118
114
x(P)
Probability
analyzer
108
402
130
MUX
126
F(s)
120
112
VCO
110
NRZ
Data
0
104
Transition
detector
102
106
124
XOR
122
304
306
gating
circuit
302
decoder
308
310
128
control
400

Fig. 4

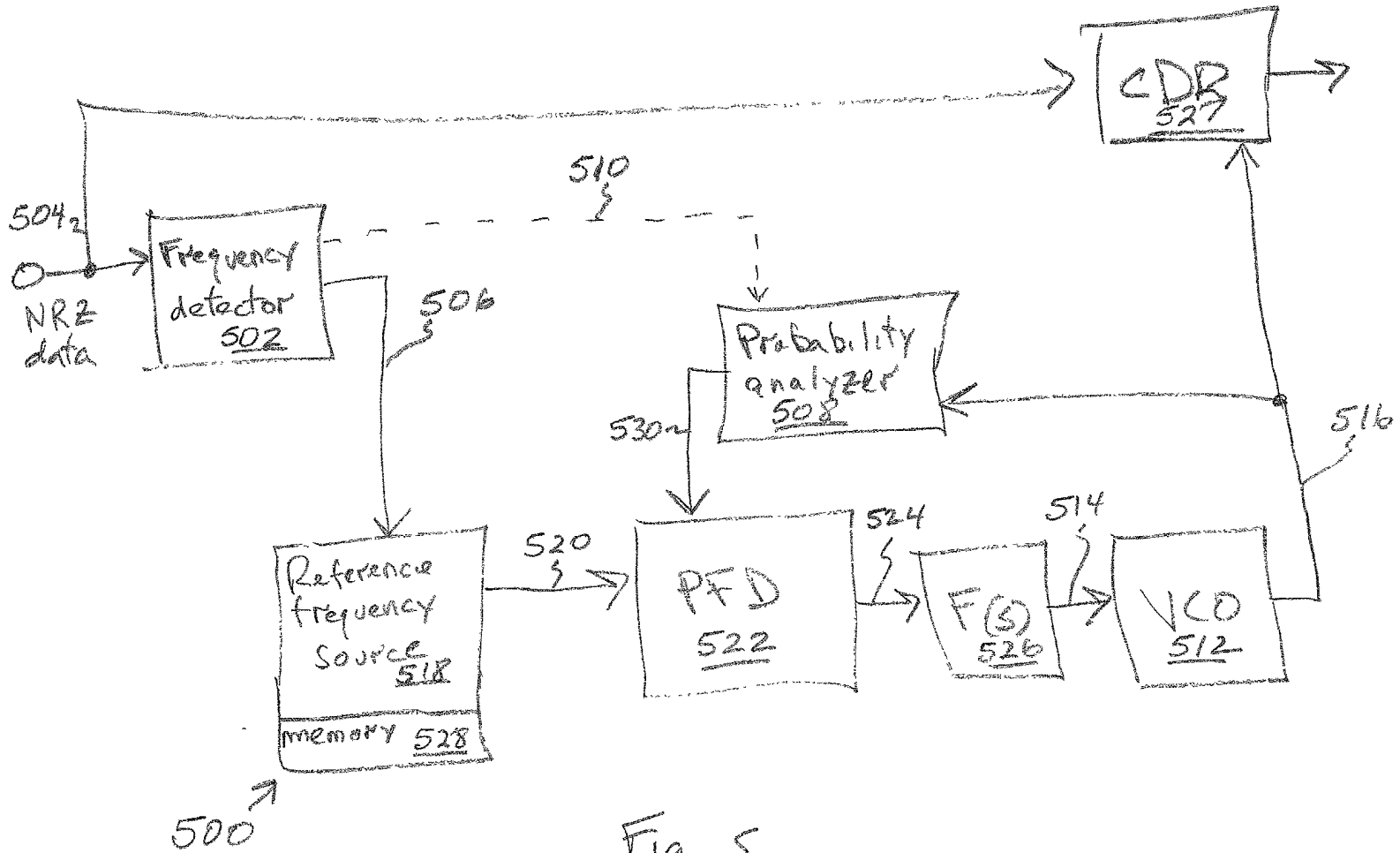
CDR
527
510
504
NRZ data
Frequency detector
502
506
Probability analyzer
508
530
516
Reference frequency source
518
memory 528
520
PFD
522
524
F(s)
526
514
VCO
512
500

Fig. 5

20220 Sheet

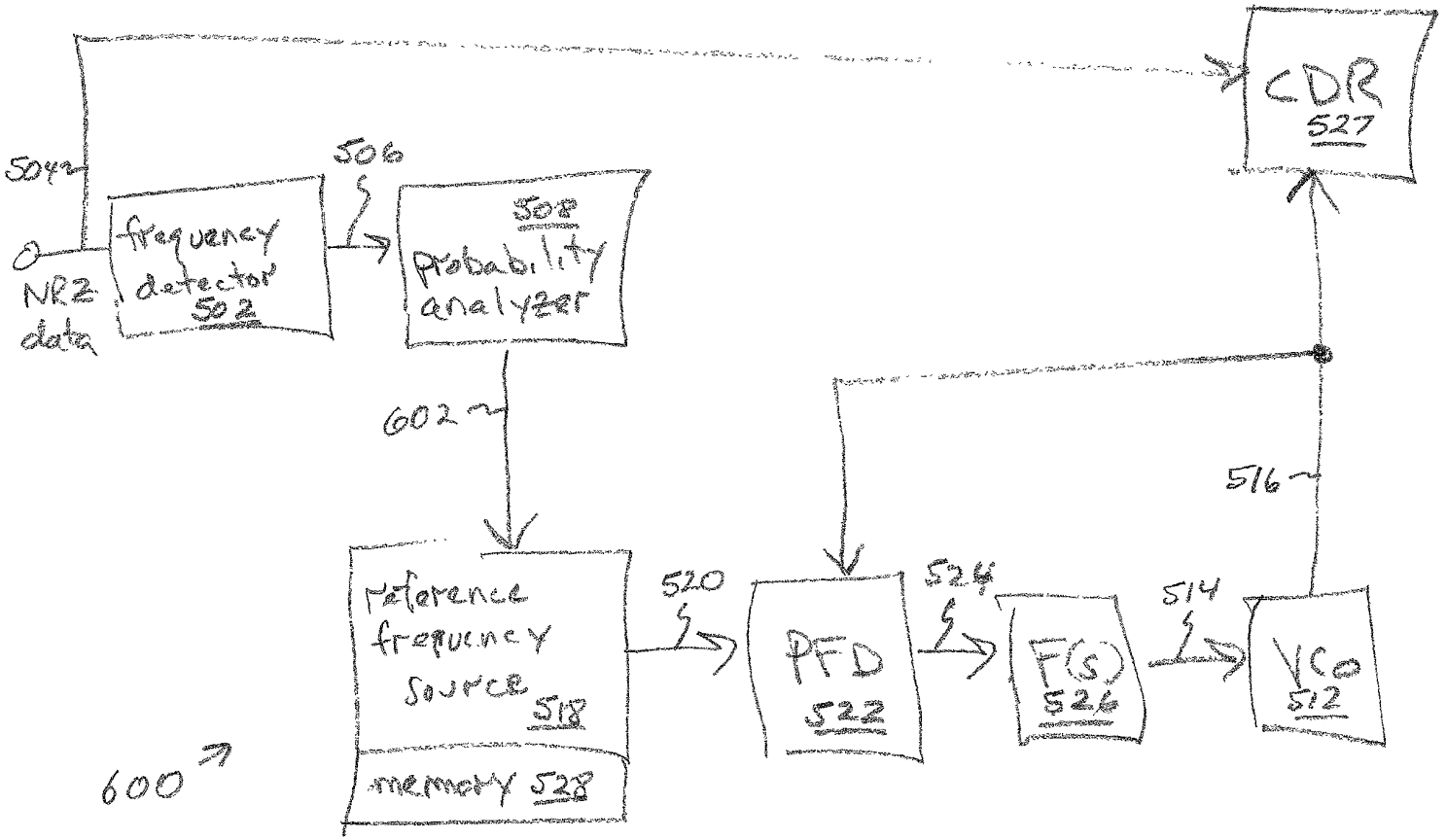

Fig. 6

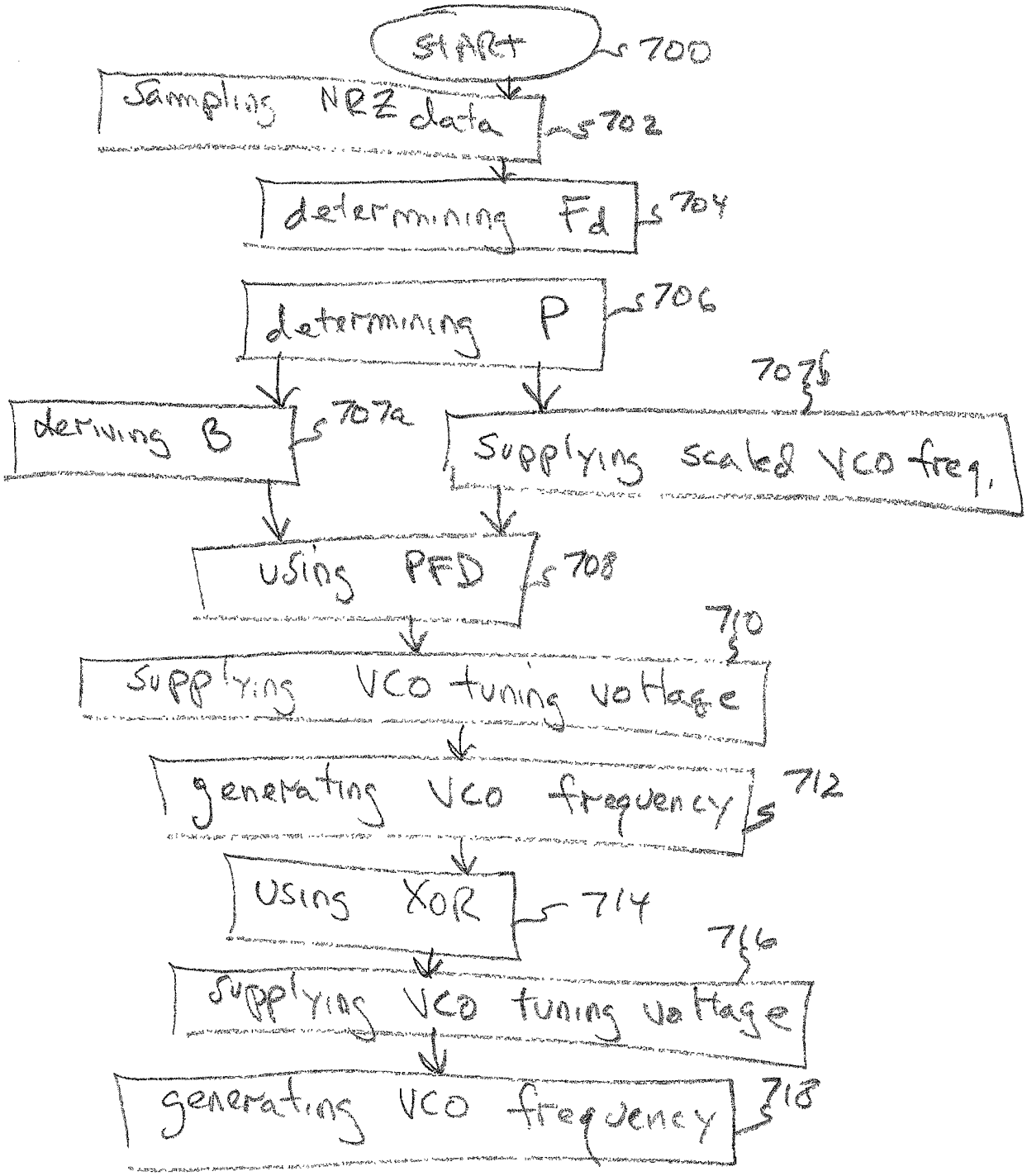
START
700
Sampling NRZ data
702
determining Fd
704
determining P
706
707a
707b
deriving B
Supplying scaled VCO freq.
using PFD
708
710
Supplying VCO tuning voltage
generating VCO frequency
712
using XOR
714
716
Supplying VCO tuning voltage
generating VCO frequency
718

Fig. 7

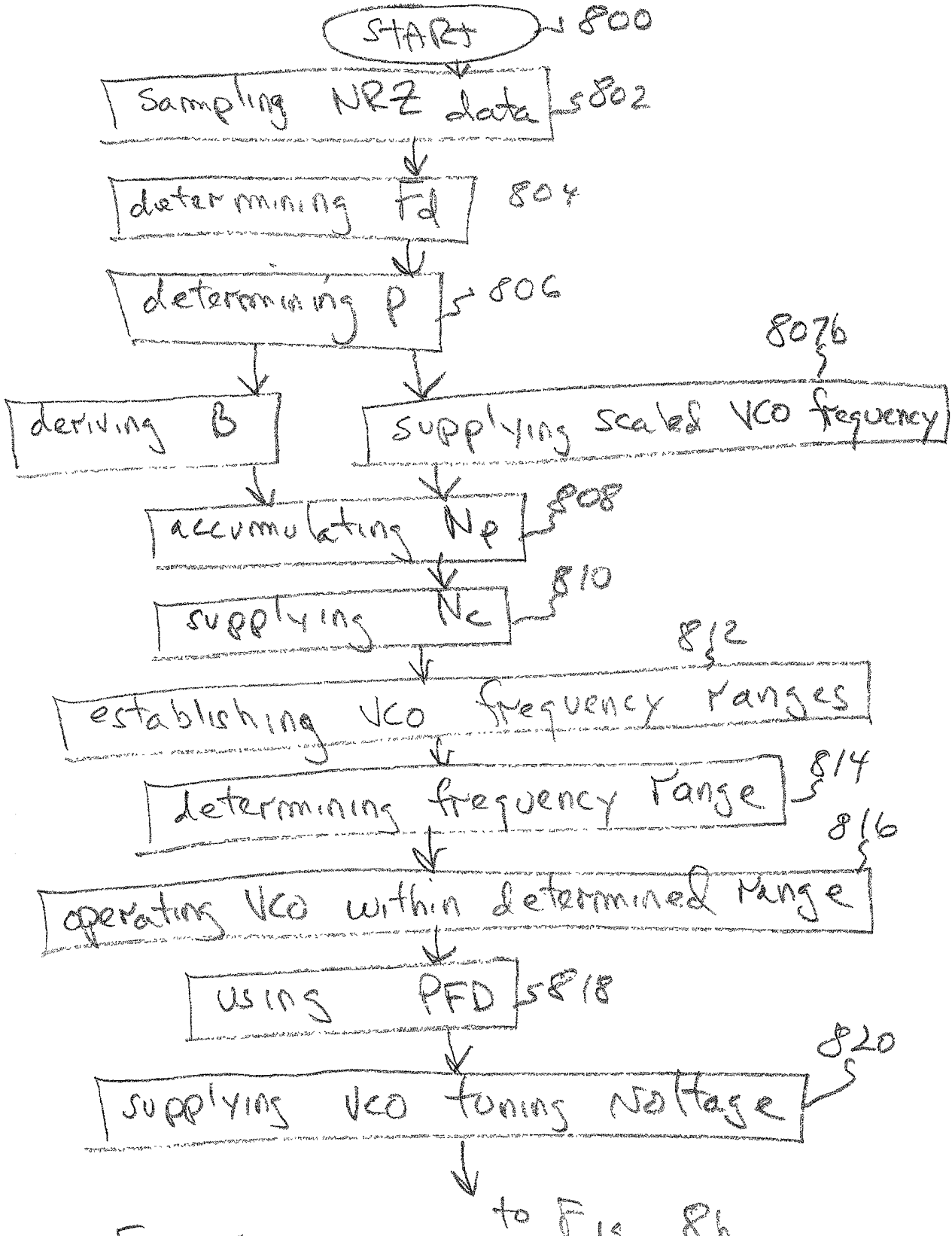
START
800
Sampling NRZ data
802
determining fd
804
determining P
806
806b
deriving B
supplying scaled VCO frequency
accumulating Np
808
supplying Nc
810
812
establishing VCO frequency ranges
determining frequency range
814
816
operating VCO within determined range
using PFD
818
820
supplying VCO tuning voltage
to Fig. 8b

Fig. 8a

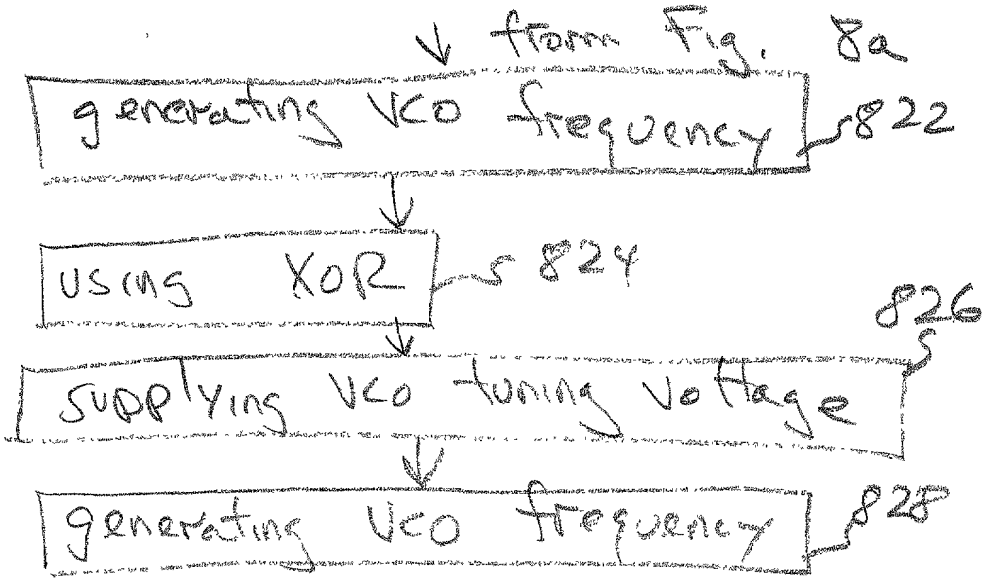
from Fig. 8a
generating VCO frequency
822
using XOR
824
826
supplying VCO tuning voltage
generating VCO frequency
828

Fig. 8b

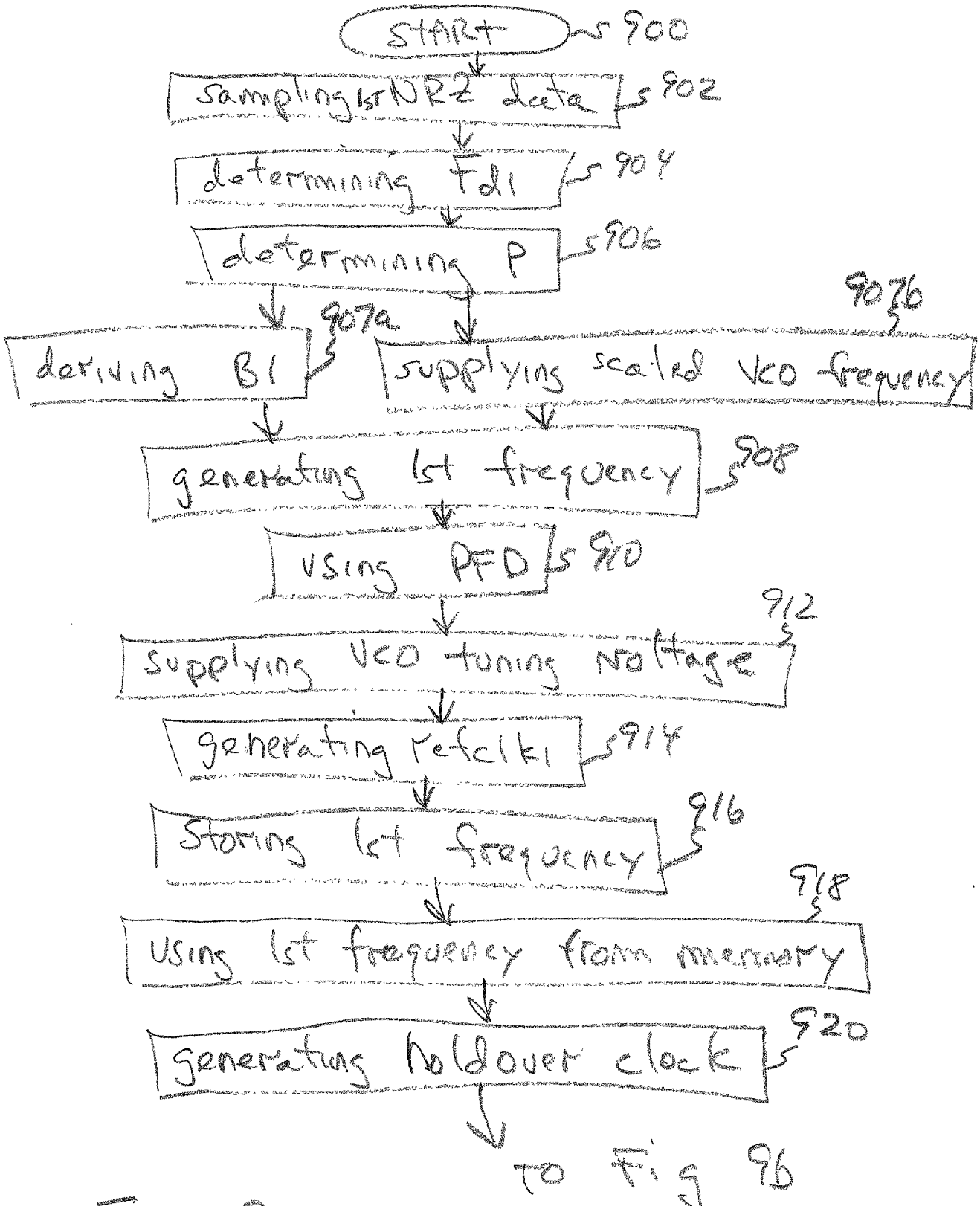
START
900
sampling 1st NRZ data
902
determining fd1
904
determining P
906
deriving B1
907a
supplying scaled VCO frequency
907b
generating 1st frequency
908
using PFD
910
supplying VCO tuning voltage
912
generating refclk1
914
storing 1st frequency
916
using 1st frequency from memory
918
generating holdover clock
920
to Fig 9b

Fig. 9a

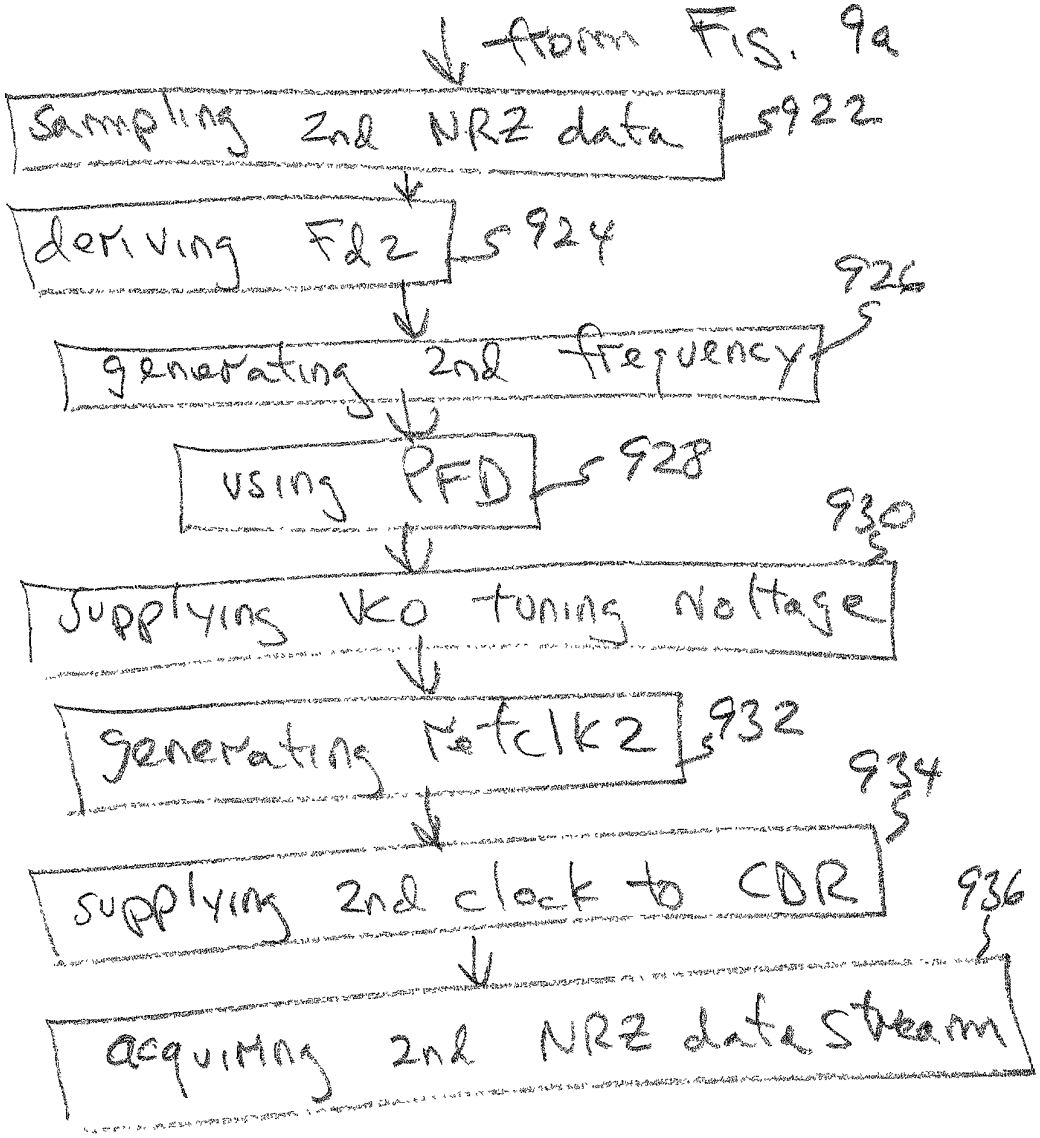
from Fig. 9a
Sampling 2nd NRZ data
922
deriving Fd2
924
generating 2nd frequency
926
using PFD
928
supplying VCO tuning voltage
930
generating Retclk2
932
supplying 2nd clock to CDR
934
acquiring 2nd NRZ data stream
936

Fig. 9b